Ocean Color Experiment Ver. 3 (OCE3)

~ Concept Presentations~

Flight Software

June 18, 2011

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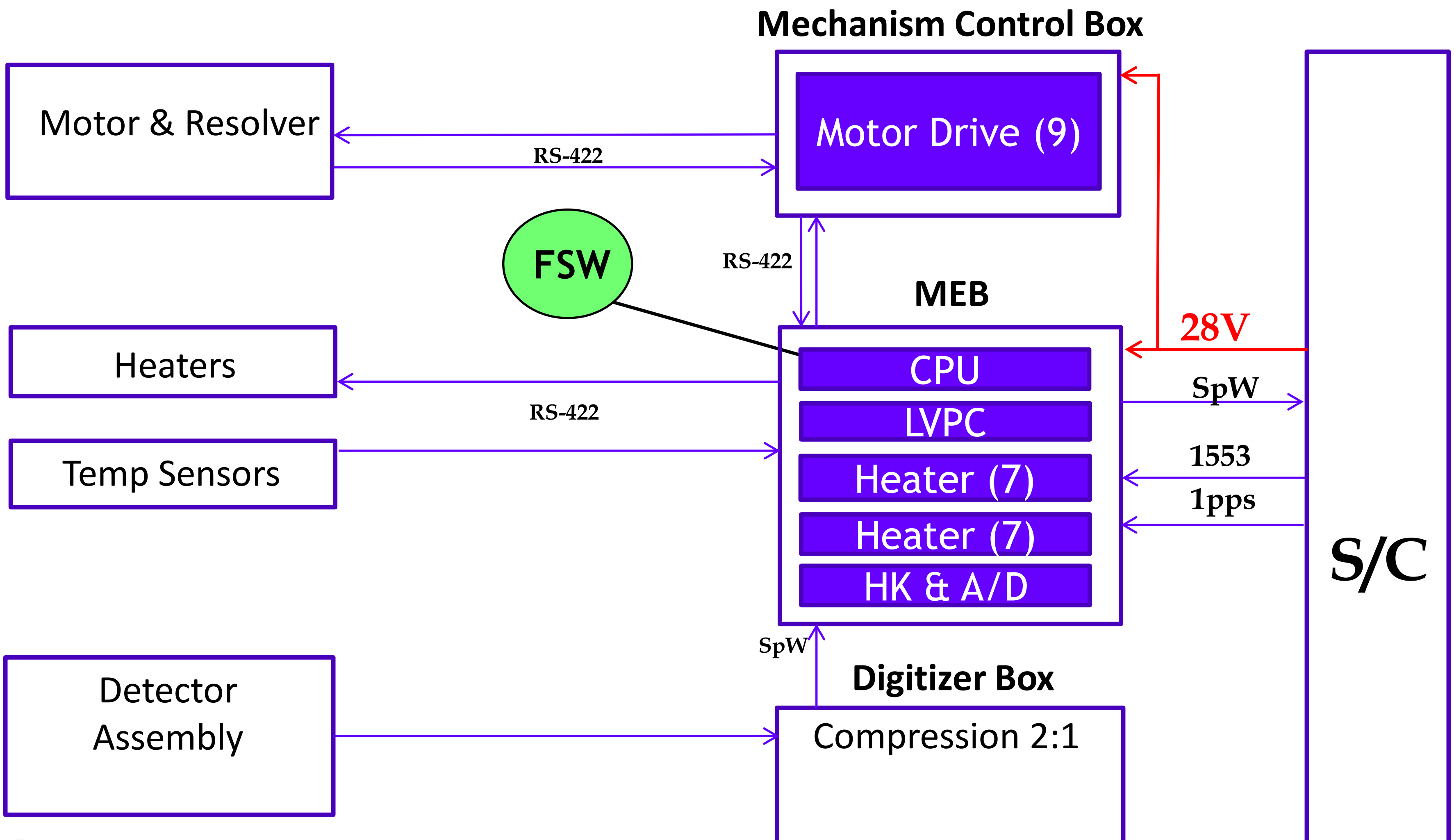
Agenda

- Electrical Block Diagrams
- Flight Software Requirements
- Conceptual Architecture
- LOC Estimate for SEER Input
- Summary
- Back up charts (estimates, testing, etc.)

Electrical Block Diagram

From Electrical Presentation



Flight Software Requirements

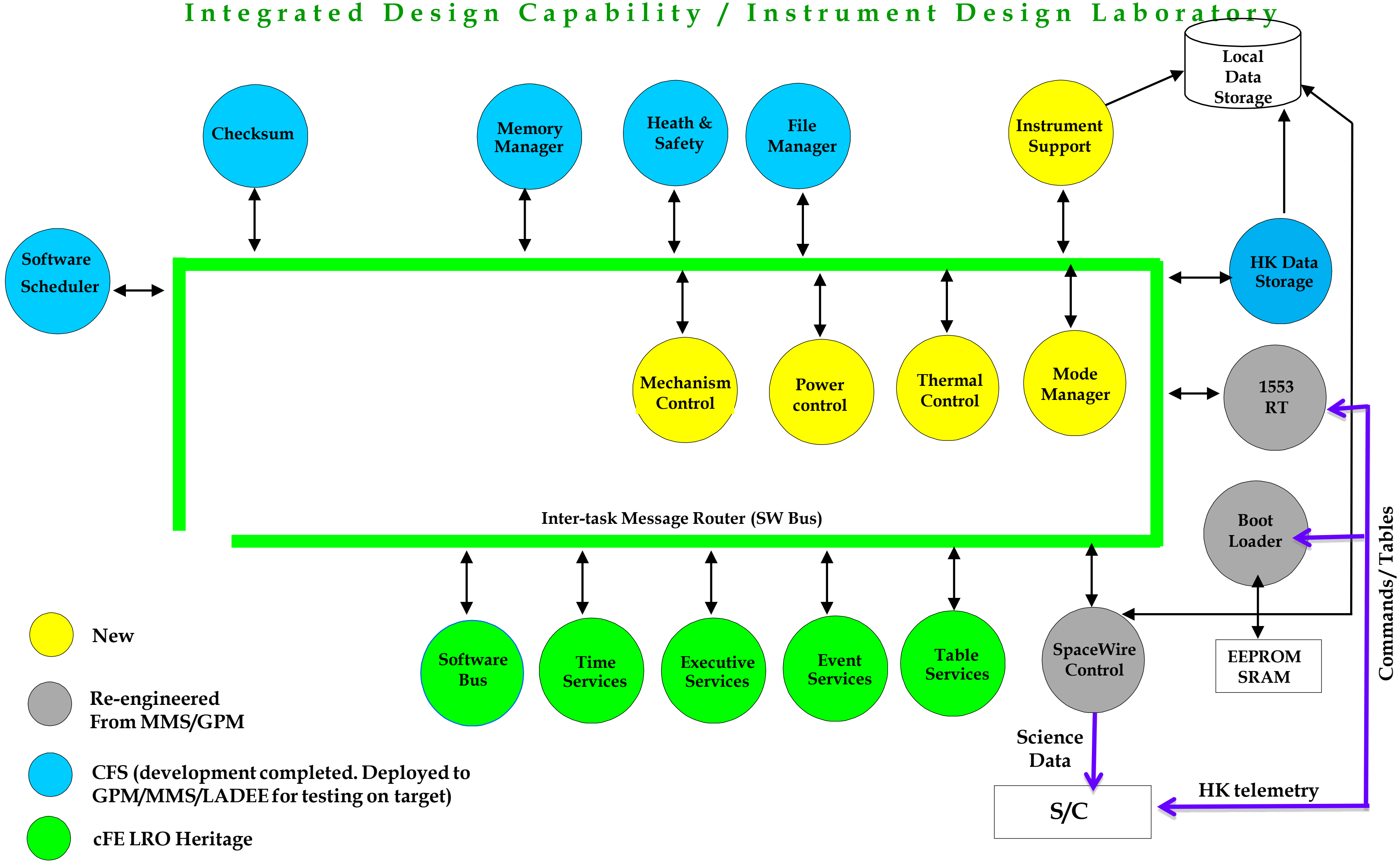
- **Driving Requirements**
  - Mode management (Boot, standby/engineering, Sun/Moon calibration, Observation, etc.)
  - Time management
    - Keeps real time synch with s/c CDH
    - Timing requirement is 1 ms accuracy
  - Instrument command & configuration
    - Command processing
    - Setup/Control digitizer boards (i.e. 12x close-loop control of integration interval)
    - Collect science/Calibration/HK data and send to S/C, multi-APID support for each data stream
  - 14x PID thermal controllers for detectors @1Hz, , +/-1 degree stability
  - Power switching services for instrument subsystem
  - Mechanisms control (5 mechanisms: Primary and ½ Angle Mirror, Momentum Compensator, Tilt, Calibration)

- **Interfaces**
  - 1PPS (S/C) – time
  - 1553 (S/C) – Instr Command and HK Tlm
  - Digital I/O (Inst) - Heaters, Thermal Sensors
  - RS-422 (Inst) – Mechanisms Control Box
  - Serial I/F (Instr) – Digitizer Box
  - SpaceWire/LVDS – science data to s/c

- **Derived**
  - Bootstrap
  - Diagnostics
  - RTEMS RTOS
  - MEB Software Management (i.e. memory load/dump, software/table updates)
  - MEB Software Health & Safety

- **NOT Requirements**
  - Science Data Processing: performed by SOC
  - Detectors readout, data integration/aggregation: performed by H/W
  - Compression: performed by H/W
  - Stored Command Processing: performed by S/C
  - Science Data Broadcasting/Recording: performed by S/C
  - Failure Detections & Corrections: performed by S/C

Flight Software Architecture

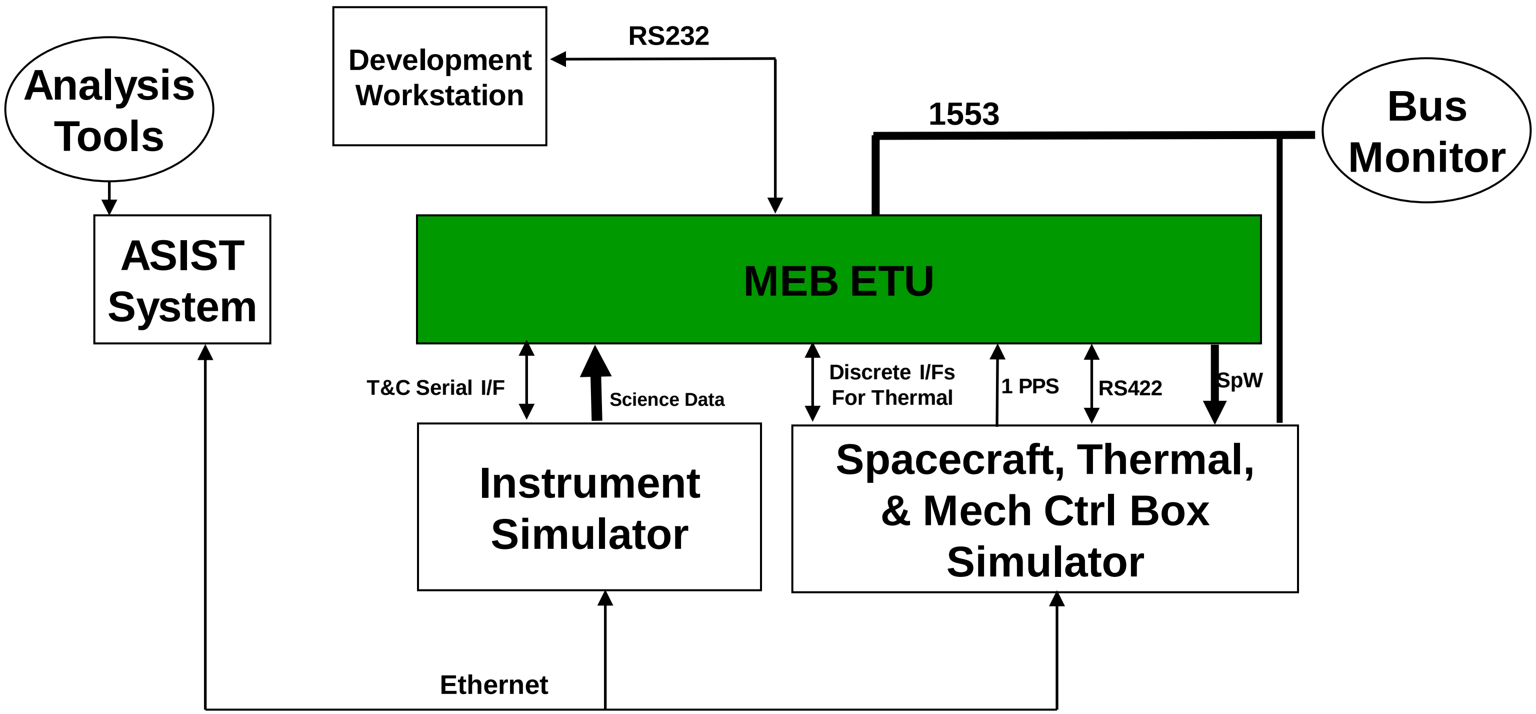


MEB Processor Utilization Estimates

	25	16	MHz Coldfire (effective rate)	BAE750(%)	12Mhz ST5/SD	60Mhz LRO
	CPU Percentages			Base Value	0.75	3.75
Component	**50 Mhz**	**32 Mhz**	**Basis of Estimate**			
cFE	0.12	0.19	LRO B2.5 Measured	0.05		0.19
HK Data Storage	0.12	0.19	LRO B2.5 Measured	0.05		0.19
Memory Manager	0.01	0.02	LRO B2.5 Measured	0.01		0.02
Health & Safety	0.17	0.26	LRO B2.5 Measured	0.07		0.26
Stored Commands	0.00	0.00	LRO B2.5 Measured	0.00		0.00
Limit Checker	0.00	0.00	LRO B2.5 Measured	0.00		0.00
Scheduler	1.46	2.29	LRO B2.5 Measured	0.61		2.29
Checksum	0.48	0.75	LRO B2.5 Measured	0.20		0.75
File Manager	0.02	0.04	LRO B2.5 Measured	0.01		0.04
Mode Manager	1.20	1.88	Estimate	0.50		1.88
SpaceWire Control	43.20	67.50	Estimate	18.00		67.50
1553 Control	6.00	9.38	Estimate	2.50		9.38
Power Control	1.20	1.88	Estimate	0.50		1.88
Instrument Support	28.80	45.00	Estimate	12.00		45.00
Solar Model	0.00	0.00	Estimate	0.00		0.00
Mechanisms Control	3.00	4.69	Estimate	1.25		4.69
Thermal Control	8.40	13.13	Estimate	3.50		13.13
Subtotal	**94.19**	**147.17**		**39.24**		

61% Margin

MEB FSW Testbed



- Top-Level Requirements:
  - Support MEB FSW development
  - Support MEB FSW build integration
  - Support MEB FSW build test

Basis of Cost Estimate

- **FSW development costs estimated using SEER: System Evaluation & Estimation of Resources**
  - NASA-wide site license for SEER managed by Langley Research Center
  - The IDL made in-house assumptions for FSW re-use and labor effort
  - IDL cannot confidently make assumptions about unknown vendor reuse libraries or control measures, or labor efforts or experience, so we apply GSFC reuse and labor assumptions
  - We assume that other centers or vendors would also have reuse libraries with similar algorithms and reuse/retest ratios
- **Grassroots test bed costs**
  - FSW test bed simulator software development 2.0 FTEs
  - FSW test bed GSE $293k
    - $6k for 3 development PC
    - $12k for 1 ASIST system
    - $15k for 1553 bus monitor
    - $20k for SpW bus monitor
    - $40k digital analyzer
    - $150k custom simulator hardware
    - $50k for software development tools (i.e. CM, DR, etc.)

MEB SLOC Estimate

Integrated Design Capability / Instrument Design Laboratory

Module Name	Environment	SW type	Approach	Development Method	Software Lines of Code (Logical))					
					Total	New	Reuse		Deleted	
(Hierarchical/Indentured list as appropriate)	(Flight, Ground)	(Control, Data mining, Database, Web, etc.)	(New, Reuse, Rehost, Maintenance, COTS I&T, etc.)				Total Reuse SLOC	% Re-engin.		% Retest needed on Reuse code
OS API & OSAL	Flight	OS/Executive	COTS I&T	OTS integration	2338	0	2338	0%	0	10
Boot Loader	Flight	Flight System	Modification, Minor	Waterfall	1868	300	1568	50%	0	100
BSP	Flight	Flight System	Reengineering, Major	Waterfall	1492	600	892	100%	0	50
Executive Services	Flight	OS/Executive	Integrate /w config	OTS integration	4737	0	4737	0%	0	10
Event Service	Flight	Flight System	Integrate /w config	OTS integration	1429	0	1429	0%	0	10
File System	Flight	Flight System	Integrate /w config	OTS integration	763	0	763	0%	0	10
Mission Config Include Files	Flight	Flight System	Reengineering, Major	OTS integration	1857	500	300	100%	1057	80
Software Bus	Flight	Flight System	Integrate /w config	OTS integration	2017	0	2017	0%	0	10
Table Service	Flight	Flight System	Integrate /w config	OTS integration	2182	0	2182	0%	0	10
Time Service	Flight	Flight System	Integrate /w config	OTS integration	1941	0	1941	0%	0	10
cFE Configuration (hdr files)	Flight	Flight System	Integrate /w config	OTS integration	226	0	226	0%	0	10
cFE platform Support Pkg	Flight	Flight System	Reengineering, Major	Waterfall	827	400	427	100%	0	100
CFS Library	Flight	Flight System	Integrate /w config	OTS integration	166	0	166	0%	0	0
Checksum	Flight	Flight System	Integrate /w config	OTS integration	2811	0	2811	0%	0	10
File Manager	Flight	Flight System	Integrate /w config	OTS integration	1664	0	1664	0%	0	10
File Commanding	Flight	Flight System	Integrate /w config	OTS integration	447	0	447	0%	0	10
Health & Safety	Flight	Flight System	Integrate /w config	OTS integration	1433	0	1433	0%	0	10
Memory Manager	Flight	Flight System	Integrate /w config	OTS integration	1927	0	1927	0%	0	10
Scheduler	Flight	Flight System	Integrate /w config	OTS integration	1067	0	1067	0%	0	10
Housekeeping	Flight	Flight System	Reengineering, Major	Waterfall	554	300	254	100%	0	50
SpaceWire Control	Flight	Flight System	Reengineering, Major	Spiral	2676	1000	1676	100%	0	100
Mechanism Control	Flight	Flight System	New	Waterfall	500	400	100	100%	0	100
Thermal Control	Flight	Flight System	Reengineering, Major	Waterfall	500	300	200	100%	0	100
Instrument Support	Flight	Flight System	Reengineering, Major	Waterfall	1000	700	300	100%	0	100
1553 Bus Control	Flight	Flight System	Reengineering, Major	Spiral	3947	1500	2447	100%	0	100
Total SLOC					40369	6000	33312			
							83%	Resuse		

Summary and Recommendations

- Line Of Code estimation shows 83% code reuse for MEB
  - High heritage based on GSFC approach
  - As noted on earlier charts, an implementation at another Center or at an experienced Vendor should also take advantage of reuse algorithms, but the specific ratio should be evaluated
- No technical show-stoppers

- Significant flight computational resources are needed If additional science data processing/reduction is to be implemented onboard (i.e. to reduce downlink bandwidth requirement)
  - Processor platform to consider:
    - SpaceCube 2.0
    - Maestro 4x4

SpaceCube 2.0 Use Cases

On-Board Processing

- Data Volume Reduction
- Image Processing
- Autonomous Operations
- Product Generation
- Event / Feature Detection
- Real-time / Direct Broadcast
- Docking / Servicing
- Compression
- Calibration / Correction
- Classification
- Inter-platform collaboration

Hybrid Science Data Processing

- CPU
- FPGA
- DSP

GSFC SpaceCube On-Board Processor

- 10x-100x computing performance
- Lower power (MIPS/watt)
- Lower cost (commercial parts)
- Radiation tolerant (not hardened)
- Software upset mitigation

Processor Comparison

	MIPS	Power	MIPS/W
MIL-STD-1750A	3	15W	0.2
RAD6000	35	10-20W	2.33 [1]
RAD750	300	10-20W	20 [2]
SPARC V8	86	1W [3]	86 [3]
LEON 3FT	60	3-5W [3]	15 [3]
GSFC SpaceCube 1.0	3000	5-15W	400 [4]
GSFC SpaceCube 2.0	5000	10-20W	500 [5]

Notes:

1 – typical, 35 MIPS at 15 watts

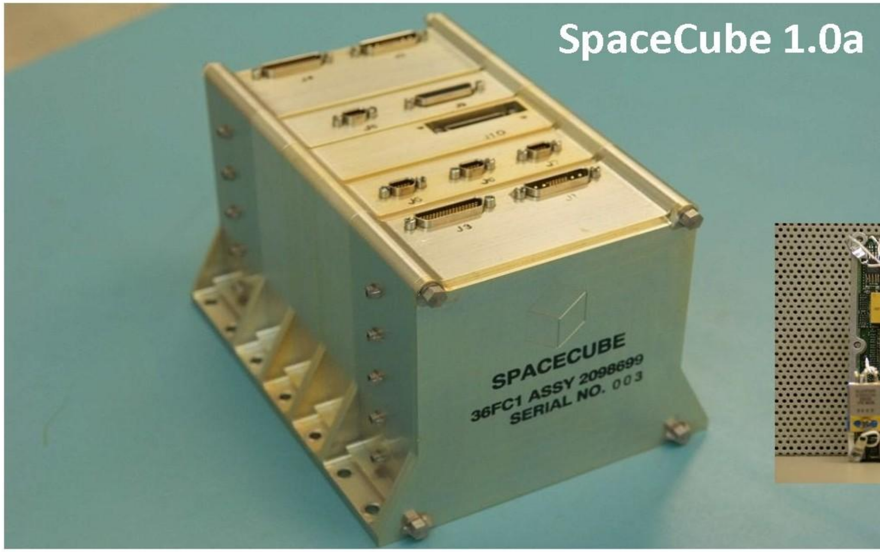
2 – typical, 300 MIPS at 15 watts

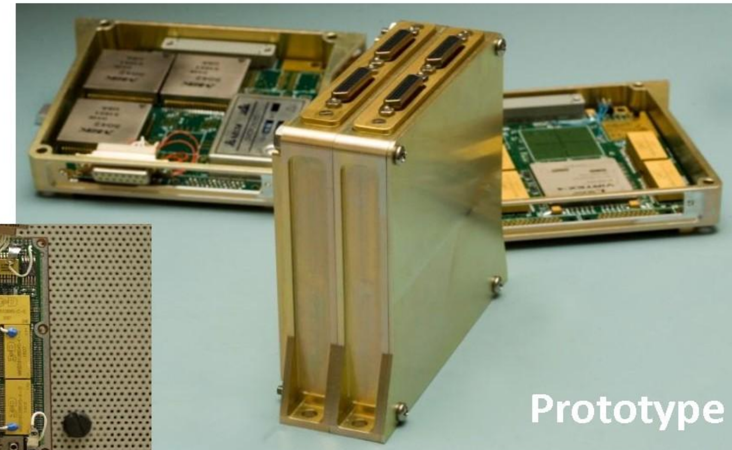
3 – processor device only … total board power TBD

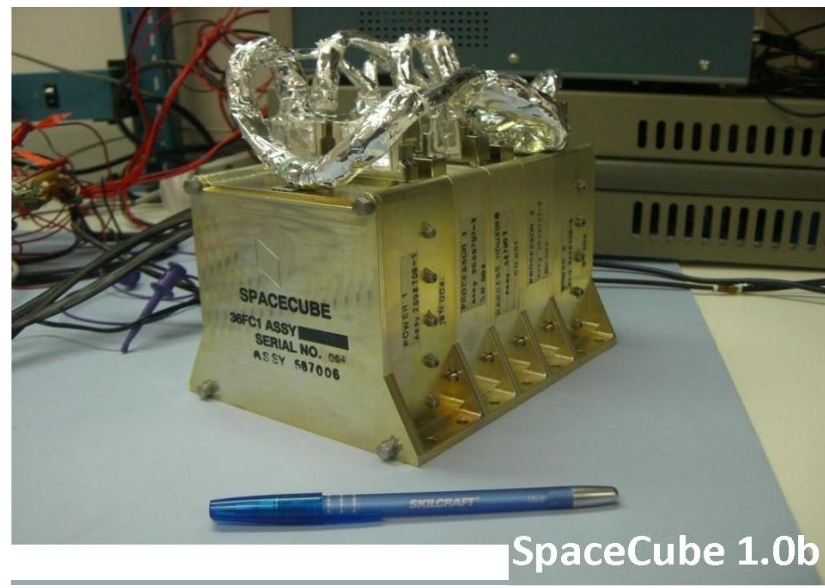
4 – 3000 MIPS at 7.5 watts (measured)

5 – 5000 MIPS at 10 watts (calculated)

Current SpaceCube Systems





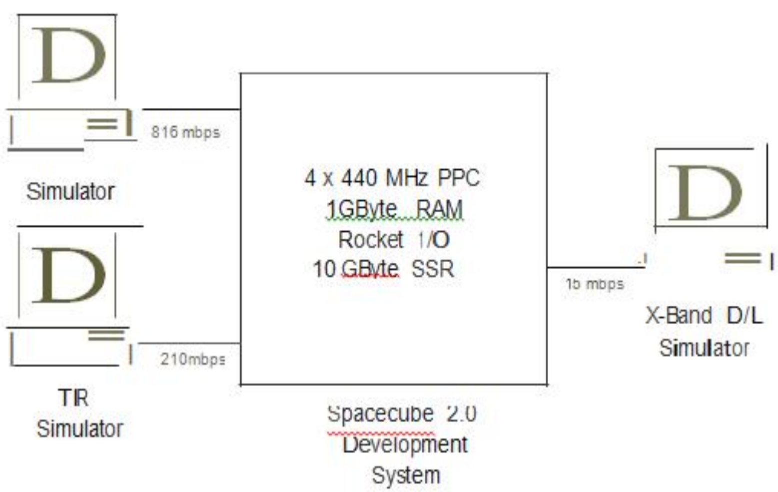


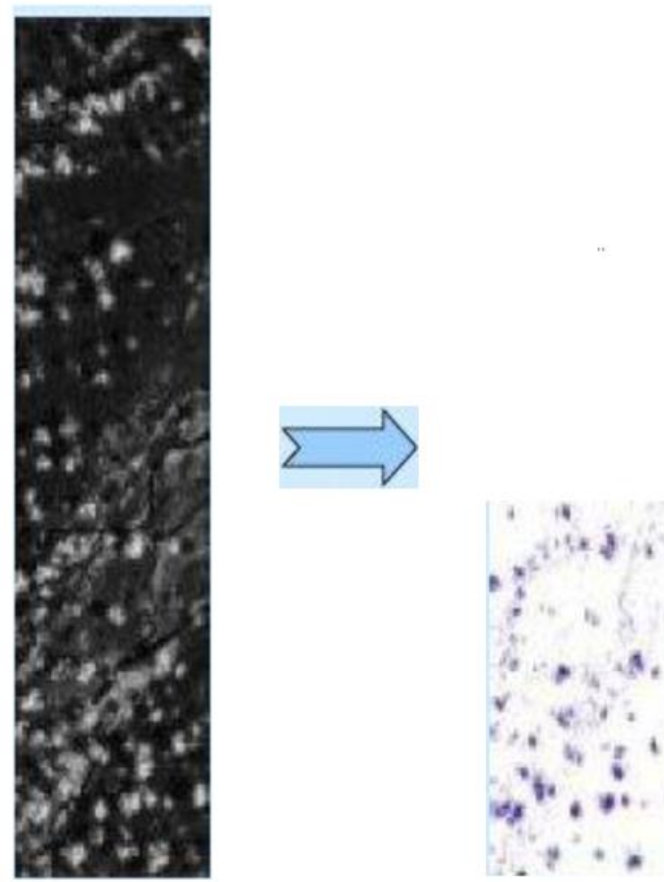
SpaceCube Family Overview

Unit	Mission	Notes	Specs	Stats	Status
SpaceCube 1.0a	Hubble Servicing Mission 4	Relative Navigation Sensors Experiment STS-125 May 2009	4"x4" card (2) Virtex4	Size: 5"x5"x7" Wt: 7.5 lbs Pwr: 37W	2009 Flight
SpaceCube 1.0b	MISSE-7 (ISS)	added RS-485, RHBS, STS-129 Nov 2009	4"x4" card (2) Virtex4	Size: 5"x5"x7" Wt: 7.5 lbs Pwr: 32W	In Flight
SpaceCube 1.0c	DEXTRE Pointing Package (ISS)	Original RNS unit, w/added 1553 & Ethernet	4"x4" card (2) Virtex4	Size: 5"x5"x7" Wt: 7.5 lbs Pwr: 40W	Final stages of Implementation
SpaceCube 1.5	SMART (DoD/ORS)	adds GigE & SATA, commercial parts, sounding rocket flight	4"x4" card (1) Virtex5	Size: 5"x5"x4" Wt: 4 lbs Pwr: < 20W	
SpaceCube 2.0	Earth/Space Science Exploration missions	Std 3U form factor, GigE, SATA, Spacewire, cPCI	4"x6" card (2) Virtex5 (1) SIRF	Size: 5"x5"x7" Wt: < 10 lbs Pwr: 20-40W	Under Development
SpaceCube 2.0 Mini	CubeSats, Sounding Rocket, UAV	"Mini" version of SpaceCube 2.0, CubeSat form factor	2.5"x2.5" card (1) Virtex5/SIRF	Size: 3.5"x3.5"x3.5" Wt: 3 lbs Pwr: <10W	

HyspiRI Demonstratoin Testbed

HyspiRI SpaceCube IPM Testbed

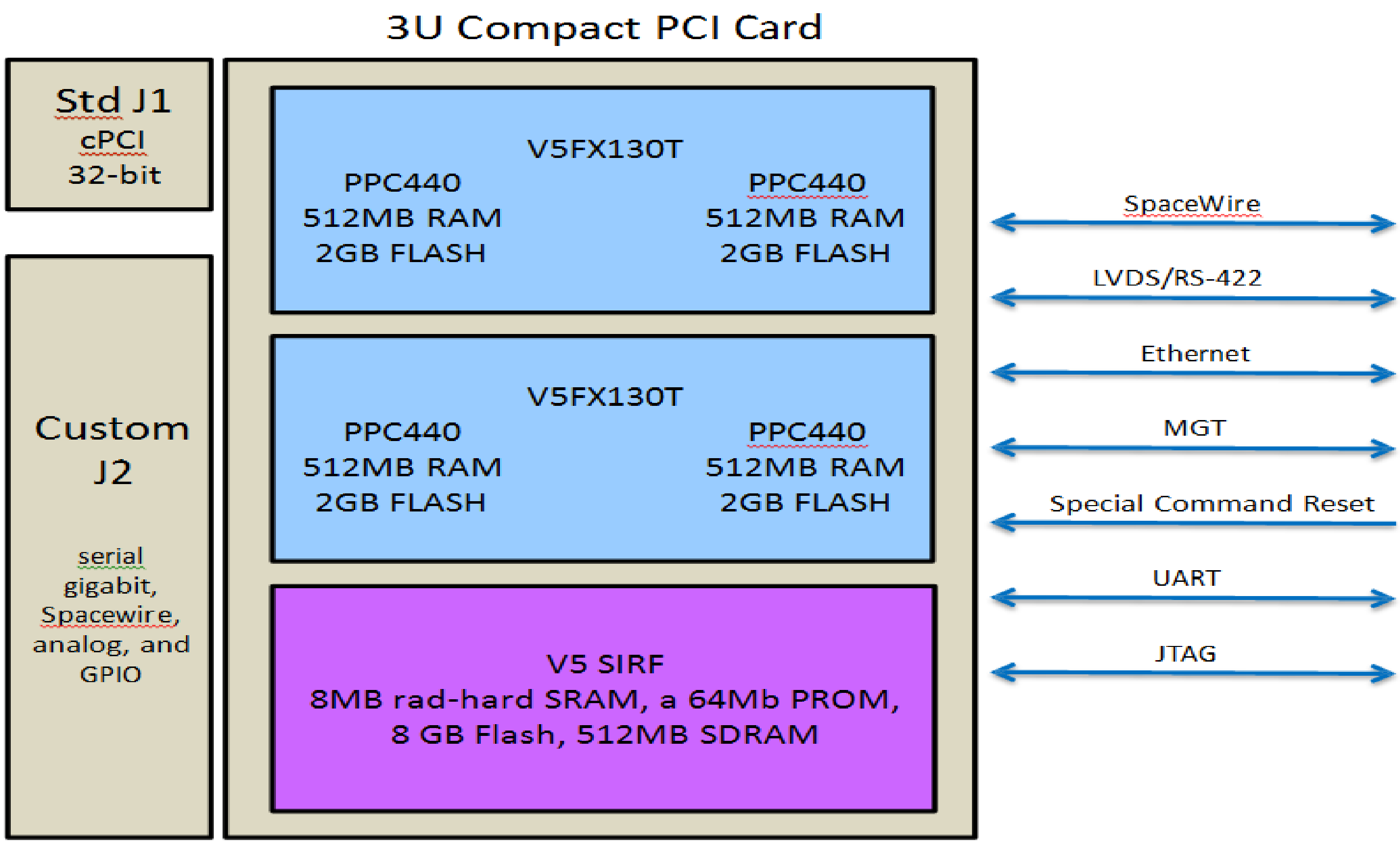




Cloud Classifier

SpaceCube 2.0 Processor Card

Integrated Design Capability / Instrument Design Laboratory



System	EDU	FLT	Notes
1.0	$500K	$850K	RNS configuration
1.5	$200K	N/A	All commercial parts
2.0	$640K	$1.1M	
Mini	$300K	$600K	Best guest for now

Backup Slides

- Development Approach
- Management Approach
- Verification & Validation

FSW Development Approach

- **Reuse LRO/GPM C&DH FSW (Med to high heritage, low risk - LRO launched 2009)**
  - LRO FSW Features (based on 582's Core Flight Executive)
    - Developed using FSW best practices consistent w/NPR 7150.2
    - Onboard file systems and associated file transfer mechanisms
    - Onboard networks with standard interfaces
    - Standard application interfaces (API) for ease of development and rapid prototyping
    - Dynamic application loading, middleware (SB) provide dynamic cmd/tlm registration
    - POSIX APIs and open source Integrated Development Environment
  - Benefits
    - Will enable parallel collaborative development and system interoperability
    - Will automate many previously manual development activities
    - Will simplify technology infusion and system evolution during development and on-orbit
    - Will enable rapid deployment of low cost, high quality mission software

- **Reengineer LRO/GPM FSW for all mission specific components**
  - Mission-specific ops concept support, thermal electronics, etc.

Management Approach

- **Product Development Process Will Comply with NPR 7150.2 (NASA Software Engineering Requirements and GOLD Rule)**
- **Development**
  - Product Development Plan per 582 branch standards, approve by Branch & Project
  - Detailed FSW development schedule integrated with project & subsystems schedules
  - Requirements management using MKS tool
  - Monthly PSR with AETD & project; branch status reviews
  - Weekly system engineering meetings, FSW team meetings
  - FSW Design & Code reviews
  - Major milestones (SCR, PDR, CDR, etc)
- **Configuration Management**
  - FSW CM Plan per 582 branch standards, approve by Branch & Project
  - Commercial CM tool (i.e., MKS) to manage source codes and document
  - Proposed FSW changes affecting missions requirements, cost and/or schedule will be forwarded to Project level CCB
- **Test Plan**
  - FSW Test Plan per 582 branch standards, approve by Branch & Project

FSW Verification and Validation

- **Unit Test**
  - Done by developers using PC tools
  - Follow Branch 582 Unit Level Test Standard - Tailored
  - Includes Path testing, Input/Output testing, Boundary testing, and Error Reporting verification
  - Occasionally BB H/W is required to verify H/W I/F
- **Build Integration Test**
  - Done by developers to verify that the FSW performs properly on the BB H/W in the FSW testbeds using embedded system tools
  - First level functionality ensured for integrated software
  - Build Test Team to assist in GSE I/F checkout
- **Build Verification Test**
  - Done by independent test team with Science Team support on the BB H/W in the FSW testbeds using embedded system tools
  - Test each requirement in the Flight Software Requirements documents (where possible at the build level)
  - Use test scenarios to test requirements in both a positive and negative fashion.
  - Scenarios constructed to combine requirements that are logically connected to create a test flow.
  - Automation to be utilized as much as possible
  - Requirements Traceability Matrix maintained